UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,735	08/07/2001	Eric Anderson	10010954-1	2921

7590 06/03/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
EHICHIOYA, FRED I	

ART UNIT	PAPER NUMBER
2172	4

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,735	ANDERSON, ERIC	
	Examiner	Art Unit	
	Fred I. Ehichioya	2172	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 25, and 30 - 43* is/are rejected.

7)☒ Claim(s) *26 - 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The rejection of claims 1 – 34 under the second paragraph of 35 U.S.C. 112 has been withdrawn as necessitated by amendment.
2. Applicant adds new claims 35 - 43
3. Claims 1 – 43 are pending in this Office Action.

Claim Objections

4. Claims 26, 27, 28 and 29 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 6, 7, 8, 9, 10, 11 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,230,151 issued to Rakesh Agrawal et al (hereinafter "Agrawal") in view of USPN 6,411,922 issued to Douglas Patrick Clark et al (hereinafter "Clark").

Regarding claim 1, Agrawal teaches an apparatus for data store assignment for a data storage system design, comprising:

a data structure stored in computer-readable memory, the data structure having a plurality of nodes, at least some of the nodes each representing a physical data storage device having respective attributes (see Fig.3);

representations of a plurality of data stores, each data store having respective requirements (see column 1, lines 40 – 65).

Agrawal does not explicitly teach solver process.

However, Clark teaches a solver process stored in computer-readable memory for assigning the representations of data stores to the data structure based on comparisons of the attributes of the nodes to the requirements of the data stores wherein the solver process makes a first assignment of a fast store and determines a first metric representative of how well the first assignment meets one or more goals for the data storage system and wherein the solver makes a second assignment of the fist store and determines a second metric representative of how well the second assignment meets the one or more goals and wherein the solver selects one of the first assignment and the second assignment based on the first and second metrics (see column 8, lines 54 - 67 and column 9, lines 31 – 64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teaching of Clark with the teaching of Agrawal wherein solver is used to solve resource optimization problems. The motivation is that this solver problem solving process provides problem modeler that requires less user skill.

Regarding claim 6, Clark teaches when the solver process assigns all of the stores to the data structure, the data structure represents a first design for the data storage system and wherein the solver determines a metric representative of how well the first design meets the one or more goals for the data storage system (see column 8, lines 54 – 67 and column 9, lines 31 – 64).

Regarding claim 7, Clark teaches the solver process reassigns at least one of the stores to the data structure thereby forming a second design for the data storage system and wherein the solver determines a metric representative of how well the second design meets the one or more goals for the data storage system (see column 8, lines 54 – 67 and column 9, lines 31 – 64).

Regarding claim 8, Clark teaches the solver process selects one of the first design and the second design based on the first and second metrics (see column 5, lines 28 – 38).

Regarding claim 9, Agrawal teaches the solver process reassigns a plurality of the stores to the data structure to form the second design (see column 9, lines 11 – 24).

Regarding 10, Clark teaches the solver process reassigns some of the stores to the data structure by removing all of the stores assigned to a particular one of the data storage devices (see column 6, lines 1 – 37).

Regarding claim 11, Agrawal teaches the plurality of nodes are arranged in a hierarchy (see Figs. 8 and 9; and column 7, lines 10 – 67).

Regarding claim 35, Clark teaches one or more of said comparisons do not indicate compatibility, the solver process adds one or more additional nodes to the data structure (see column 8, lines 54 – 67).

7. Claims 2, 3, 4, 5, 12, 16, 18, 19, 20, 36, 37, 38 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal in view of Clark and further in view of USPN 6,473,884 issued to Malay Kumar Ganai et al (hereinafter "Ganai").

Regarding claim 2, Clark teaches solve process. Agrawal or Clark does not explicitly teach assignments.

However Ganai teaches wherein the solver process compares the requirements of the store to the attributes of one or more of the data storage devices and when the comparison indicates compatibility, the solver process makes the first assignment of the store (see column 4, lines 17 – 44).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teaching of Ganai with the teaching of Agrawal and Clark wherein the values of the nodes are assigned. The combination thus produces a solver that is used for resource assignment. The motivation is that this solver problem solving process provides problem modeler that requires less user skill.

Regarding claim 3, Agrawal teaches wherein the plurality of nodes are arranged in a hierarchy (see Figs. 8 and 9; and column 7, lines 10 – 67).

Regarding claim 4, Ganai teaches wherein the solver process makes at least one additional assignment of the data store (see column 4, lines 17 – 44).

Regarding claim 5, Ganai teaches wherein the solver process selects one of the first assignment, the second assignment and the at least one additional assignment based on how well goals for the data storage system are met (see column 3, lines 22 – 43).

Regarding claim 12, Ganai teaches wherein one or more of said comparisons do not indicate compatibility, the solver process modifies one or more of the attributes of one or more of the data storage devices (see column 3, lines 39 – 43).

Regarding claim 16, Clark teaches when the solver process assigns all of the stores to the data structure, the data structure represents a first design for the data storage system and wherein the solver determines a metric representative o f how well the first design meets the one or more goals for the data storage system (see column 8, lines 54 – 67 and column 9, lines 31 – 64).

Regarding claim 18, Ganai teaches wherein the solver process reassigns some of the stores to the data structure thereby forming a second design for the data storage system and wherein the solver determines a metric representative of how well the second design meets the one or more goals for the data storage system (see column 4, lines 17 – 44).

Regarding claim 19, Clark teaches the solver process selects one of the first design and the second design based on the first and second metrics (see column 5, lines 28 – 38).

Regarding claim 20, Ganai teaches the solver process reassigns some of the stores to the data structure by removing all of the stores assigned to a particular one of the data storage devices (see column 4, lines 17 – 44).

Regarding claim 36, Ganai teaches the solver process assigns at least some of the stores to the data structure and then removes at least one of the stores from the data structure (see column 4, lines 17 – 25).

Regarding claims 37 and 38, Agrawal teaches the solver process removes a storage device from the design when no stores are assigned to the storage device (see column 12, lines 11 – 16).

Regarding claim 41, Clark teaches the solver process removes a storage device from the design when no stores are assigned to the storage device (see column 9, lines 31 – 64).

8. Claims 13, 14, 15, 17, 39, 40, 42, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal in view of Ganai.

Regarding claim 13, Agrawal teaches an apparatus for data store assignment for a data storage system design, comprising:

a data structure stored in computer-readable memory, the data structure having a plurality of nodes, at least some of the nodes each representing a physical data storage device and having respective attributes (see Fig.3);

representations of a plurality of data stores, each data store having respective requirements (see column 1, lines 40 – 65 and column 12, lines 11 – 33).

Agrawal does not explicitly teach solver process.

Ganai teaches a solver process stored in computer-readable memory for assigning the representations of data stores to the nodes wherein the solver process compares the requirements of a store to the attributes of one or more of the data storage devices and when the comparison indicates compatibility, the solver process makes a first assignment of the store and when the comparison does not indicate compatibility, the solver process modifies one or more of the attributes of one or more of the data storage devices (see column 3, lines 22 – 43 and column 4, lines 17 – 44).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teaching of Ganai with the teaching of Agrawal wherein solver is used to solve resource optimization problems. The motivation is that this solver problem solving process provides problem modeler that requires less user skill.

Regarding claim 14, Ganai teaches the solver process makes at least one additional assignment of the data store (see column 4, lines 17 – 44).

Regarding claim 15, Ganai teaches the solver process selects one of the first assignment and the at least one additional assignment based on how well one or more goals for the data storage system are met (see column 3, lines 22 – 43).

Regarding claim 17, Agrawal teaches wherein the plurality of nodes are arranged in a hierarchy (see Figs. 8 and 9; and column 7, lines 10 – 67).

Regarding claim 39, Ganai teaches the solver process assigns at least some of the stores to the data structure and then removes at least one of the stores from the data structure (see column 4, lines 17 – 25).

Regarding claim 40, Agrawal teaches the solver process removes a storage device from the design when no stores are assigned to the storage device (see column 12, lines 11 – 16).

Regarding claim 42, Agrawal teaches an apparatus for data store assignment for a data storage system design, comprising:

a data structure stored in computer-readable memory, the data structure having a plurality of nodes, at least some of the nodes each representing a physical data storage device and having respective attributes (see Fig.3);

representations of a plurality of data stores, each data store having respective requirements (see column 1, lines 40 – 65 and column 12, lines 11 – 33).

Agrawal does not explicitly teach solver process.

Ganai teaches a solver process stored in computer-readable memory for assigning the representations of data stores to the nodes wherein the solver process compares the requirements of a store to the attributes of one or more of the data storage devices and when the comparison indicates compatibility, the solver process makes a first assignment of the store and when the comparison does not indicate compatibility, the solver process adds one or more additional nodes to the data structure (see column 3, lines 22 – 43 and column 4, lines 17 – 44).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teaching of Ganai with the teaching of Agrawal wherein solver is used to solve resource optimization problems. The motivation is that this solver problem solving process provides problem modeler that requires less user skill.

Regarding claim 43, Ganai teaches the solver process makes a first assignment of the store to the one or more additional nodes (see column 4, lines 17 – 44).

9. Claims 21, 23, 24, 25, 30, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ganai in view of Clark.

Regarding claim 21, Ganai teaches a method of data store assignment for a data storage system design, comprising:

providing a data structure stored in computer-readable memory, the data structure having a plurality of nodes, at least some of the nodes each representing a physical data storage device having respective attributes (see column 3, lines 3 – 32);

providing a representation of a first data store having requirements (see column 3, lines 32 – 35);

comparing the requirements for the data store to attributes of devices in the data structure (see column 3, lines 3 - 6;

making a first assignment of the representation of the first data store to the data structure based on results of said comparing (see column 3, lines 22 – 43);

making a second assignment of the representation of the data store based on said results of said comparing (see column 4, lines 7 – 16).

Ganai does not explicitly teach determining metrics.

Clark teaches determining a first metric for the first assignment according to how well the first assignment meets one or more goals for the data storage system (see column 8, lines 54 – 67);

determining a second metric for the second assignment according to how well the second assignment meets the one or more goals for the data storage system (see column 9, lines 31 – 64); and

selecting the first assignment or the second assignment based on the first and second metrics (see column 9, lines 51 – 64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teaching of Clark with the teaching of Ganai wherein problem solver determines metrics and metric relationship. The motivation is that metric generator periodically or continuously monitors information resource to determine its current objects and the state of those objects, and then updates the metrics for solver database.

Regarding claim 23, Ganai teaches modifying the attributes of one or more of the nodes into compatibility with the requirements of the data store (see column 3, lines 22 – 43).

Regarding claim 24, Ganai teaches making at least one additional assignment of the first data store (see column 4, lines 17 – 44).

Regarding claim 25, Ganai teaches the solver process selects one of the first assignment, the second assignment and the at least one additional assignment based on how well goals for the data storage system are met (see column 3, lines 22 – 43).

Regarding claim 30, Ganai teaches a method of data store assignment for a data storage system design, comprising:

providing a data structure stored in computer-readable memory, the data structure having a plurality of nodes, at least some of the nodes each representing a physical data storage device having respective attributes (see column 3, lines 3 – 32);

providing representations of a plurality of data stores, each having requirements (see column 3, lines 32 – 35);

comparing the requirements for each data store to attributes of devices in the data structure (see column3, lines 3 – 6);

making a first assignment of the representations of each of the plurality of stores to the data structure based on results of said comparing (see column 3, lines 22 – 43);

making a second assignment of the representations of each of the plurality of data stores based on said results of the said comparing (see column 4, lines 7 – 16);

Ganai does not explicitly teach determining metrics.

Clark teaches determining a first metric for the first assignment according to how well the first assignment meets one or more goals for the data storage system (see column 8, lines 54 – 67);

determining a second metric for the second assignment according to how well the second assignment meets the one or more goals for the data storage system (see column 9, lines 31 – 64); and

selecting the first assignment or the second assignment based on the first and second metrics (see column 9, lines 51 – 64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teaching of Clark with the teaching of Ganai wherein problem solver determines metrics and metric relationship. The motivation is that metric generator periodically or continuously monitors information resource to determine its current objects and the state of those objects, and then updates the metrics for solver database.

Regarding claim 32, Clark teaches when said comparing does not indicate compatibility, modifying one or more of the nodes (see column 8, lines 54 – 67).

Regarding claim 33, Ganai teaches said modifying comprising expanding data storage capacity of the one or more nodes (see column 4, lines 40 – 42).

10. Claims 22, 31 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ganai in view of Clark and further in view of Agrawal.

Regarding claim 22, Ganai and Clark disclose the claim subject matter as discussed in claim 1. Agrawal teaches the plurality of nodes are arranged in a hierarchy (see Figs. 8 and 9; and column 7, lines 10 – 67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine teaching of Agrawal with the teaching of Ganai and

Clark wherein data stored in the memory correspond to hierarchical nodes. The motivation is that continuously monitor of this information resource is more efficient.

Regarding claim 31, Agrawal teaches wherein the plurality of nodes are arranged in a hierarchy (see Figs. 8 and 9; and column 7, lines 10 – 67).

Regarding claim 34, Agrawal teaches said data structure further comprising representations of data storage devices that can be added to a design for the data storage system, but have not been added to the design (see column 7, lines 12 – 67).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred I. Ehichioya whose telephone number is 703-305-8039. The examiner can normally be reached on M - F 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Breene can be reached on 703-305-9790. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fred I. Ehichioya
Examiner
Art Unit 2172
May 25, 2004

SHAHID ALAM
PRIMARY EXAMINER